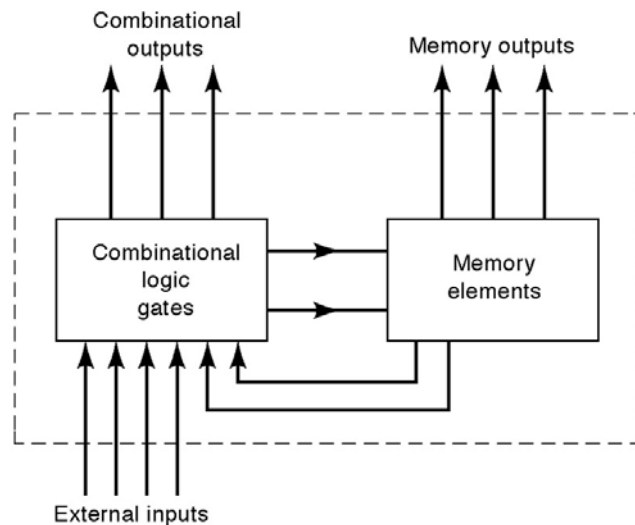# Lecture 9: Flip-flops

Professor Peter Cheung
Department of EEE, Imperial College London

(Floyd 7.1-7.4)
(Tocci 5.1-5.9)

Points Addressed in this Lecture

- Properties of synchronous and asynchronous sequential circuits
- Overview of flip-flops and latches

General digital system diagram

Properties of Sequential Circuits

- So far we have seen Combinational Logic
  - the output(s) depends only on the current values of the input variables
- Here we will look at Sequential Logic circuits
  - the output(s) can depend on present and also past values of the input and the output variables
- Sequential circuits exist in one of a defined number of states at any one time
  - they move "sequentially" through a defined sequence of transitions from one state to the next
  - The <u>output variables</u> are used to describe the state of a sequential circuit either directly or by deriving <u>state variables</u> from them

Synchronous and Asynchronous Sequential Logic

- Synchronous
  - the timing of all state transitions is controlled by a <u>common clock</u>
  - changes in all variables occur simultaneously
- Asynchronous
  - state transitions occur independently of any clock and normally dependent on the timing of transitions in the input variables
  - changes in more than one output do not necessarily occur simultaneously
- Clock
  - A clock signal is a square wave of fixed frequency
  - Often, transitions will occur on one of the edges of clock pulses
   - i.e. the rising edge or the falling edge

Flip-Flops

- Flip-flops are the fundamental element of sequential circuits
  - bistable
  - (gates are the fundamental element for combinational circuits)
- Flip-flops are essentially 1-bit storage devices
  - outputs can be set to store either 0 or 1 depending on the inputs
  - even when the inputs are de-asserted, the outputs retain their prescribed value
- Flip-flops have (normally) 2 complimentary outputs
  - Q and $\overline{Q}$
- Three main types of flip-flop
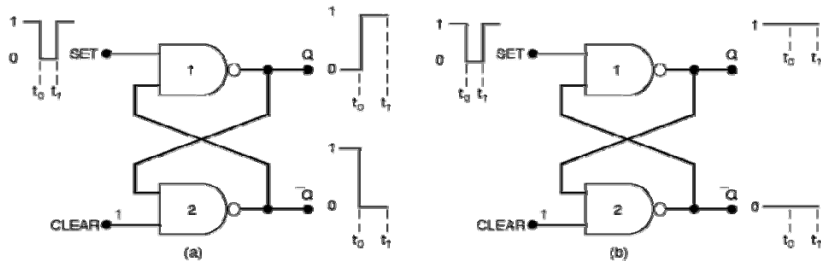 - R-S   J-K   D-type

Flip-Flop
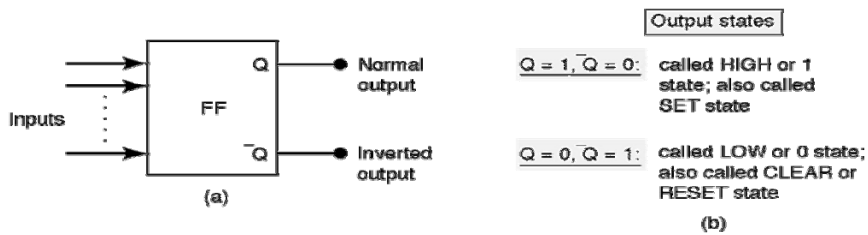
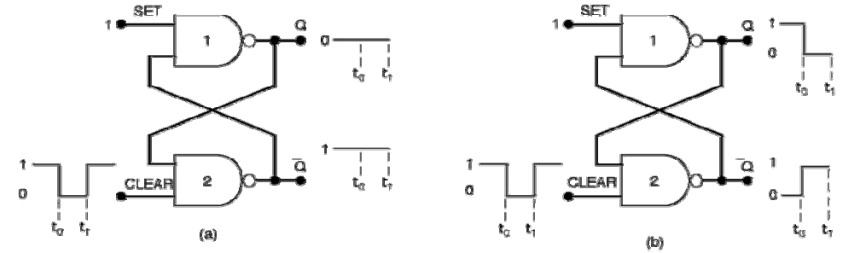**FF = latch = bistable circuit**

NAND Gate Latch
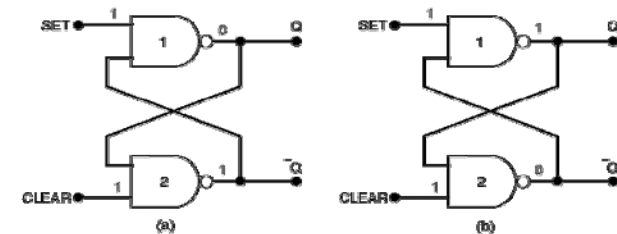
A NAND latch has two possible resting states when SET = CLEAR = 1.
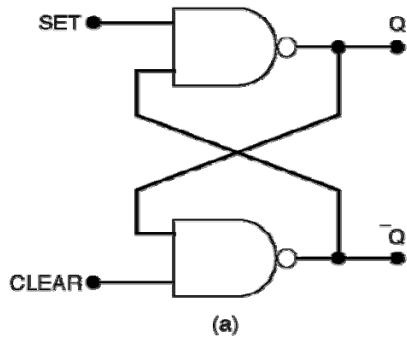
NAND Gate Latch (cont.)

Negative Pulse on SET input put the latch in a HIGH (SET) state

NAND Gate Latch (cont.)

Negative Pulse on CLEAR input put the latch in a LOW (Clear or RESET) state
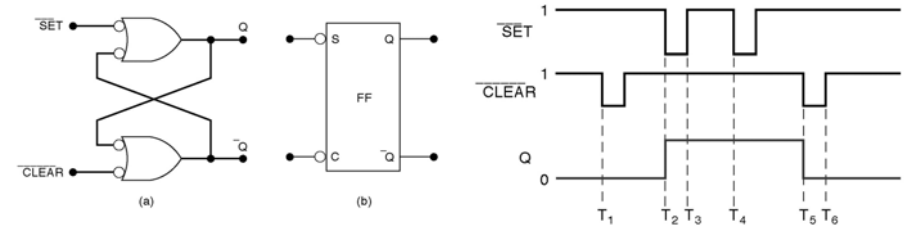
NAND Gate Latch (cont.)

Set	Clear	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid*

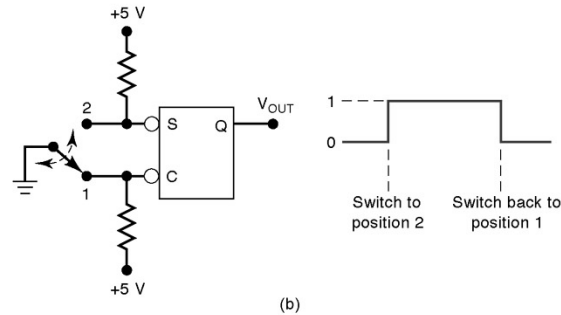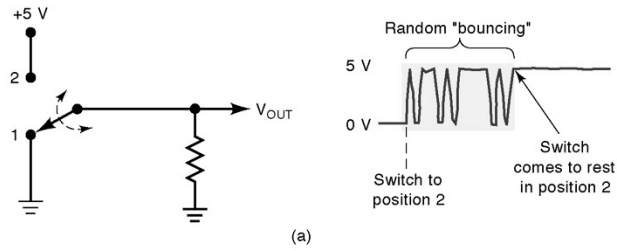*produces $Q = \overline{Q} = 1$

(b)

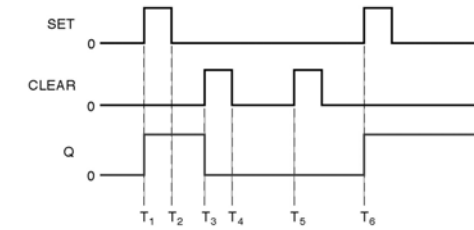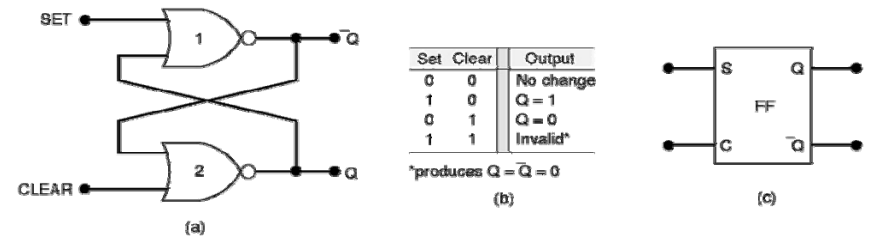**Truth table for the NAND Set-Clear (Set-Reset or SR) Latch**

Alternative representation of SR Latch

SR Latch to deglitch a switch

+5 V

(a)

Random "bouncing"

5 V

0 V

Switch comes to rest in position 2

Switch to position 2

(b)

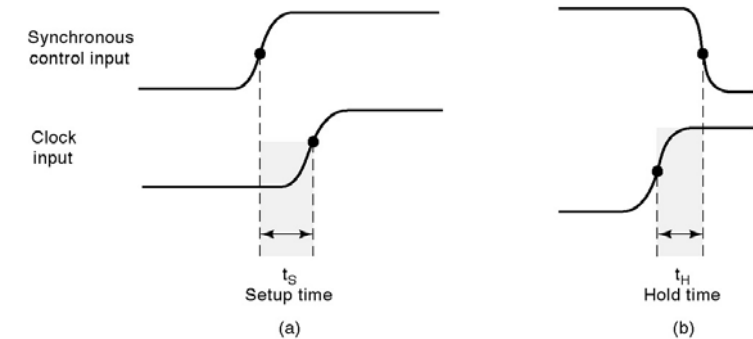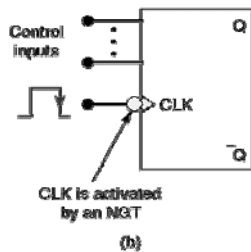+5 V

V_{OUT}

Switch to position 2

Switch back to position 1

+5 V

NOR gate Latch

* **Made of two cross-coupled NOR gates**

SET

CLEAR

(a)

Set	Clear	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*produces Q = Q̄ = 0

(b)

S　Q

FF

C　Q̄

(c)

SET

CLEAR

Q

T_1 T_2　T_3 T_4　　T_5　　T_6


Clock Signals and Clocked FFs

* **Digital systems can operate**
  - **Asynchronously: output can change state whenever inputs change**
  - **Synchronously: output only change state at clock transitions (edges)**
* **Clock signal**
  - **Outputs change state at the transition (edge) of the input clock**
  - **Positive-going transitions (PGT)**
  - **Negative-going transitions (NGT)**

Positive-going transition (PGT)　Negative-going transition (NGT)

(a) → Time

(b)

Control inputs

CLK

CLK is activated by a PGT

(a)

Control inputs

CLK

CLK is activated by an NGT

(b)

Synchronous control input

Clock input

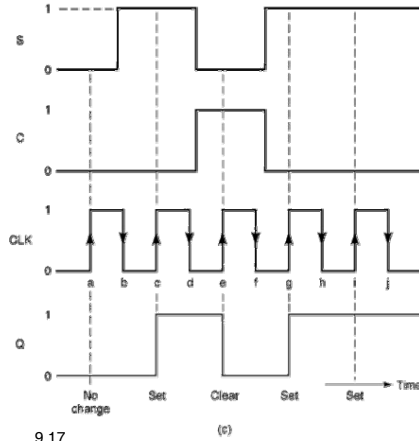t_S Setup time

(a)

t_H Hold time

(b)
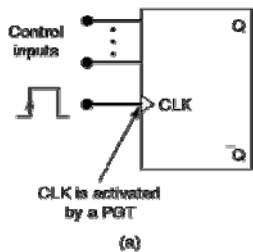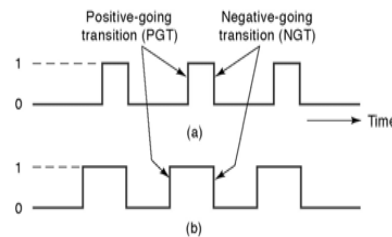
Control inputs must be held stable for (a) a time t_S prior to active clock transition and for (b) a time t_H after the active block transition.
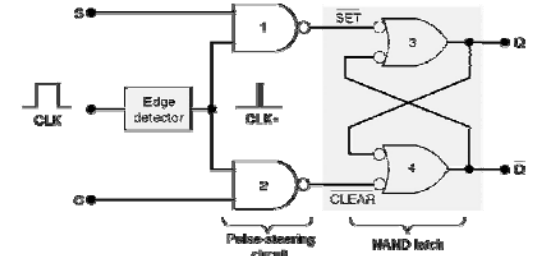
Clocked S-C FF

(a)

(b)
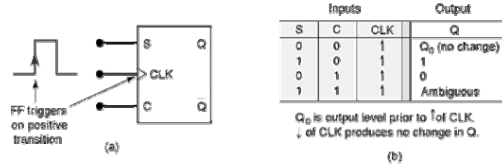
(a) Clocked S-C FF that responds only to the positive-going edge of a clock pulse;
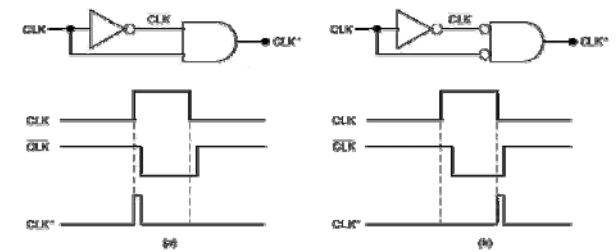(b) truth table;
(c) Typical waveforms.

(c)

Internal Circuitry of S-C FF

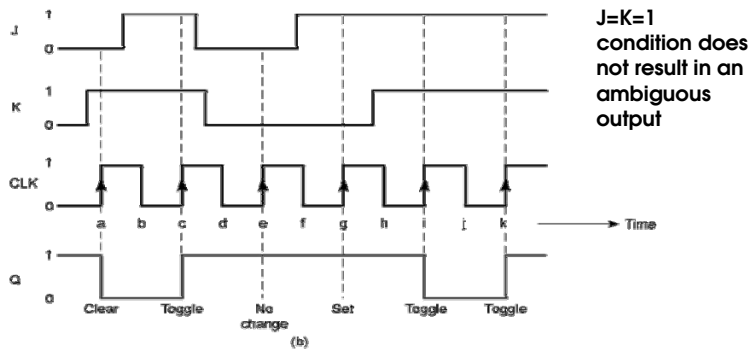Simplified version of the internal circuitry for an edge-triggered S-C FF

Implementation of edge-detector circuits used in edge-triggered FFs: (a) PGT; (b) NGT. The duration of the *CLK** pulses is typically 2-5 *ns*
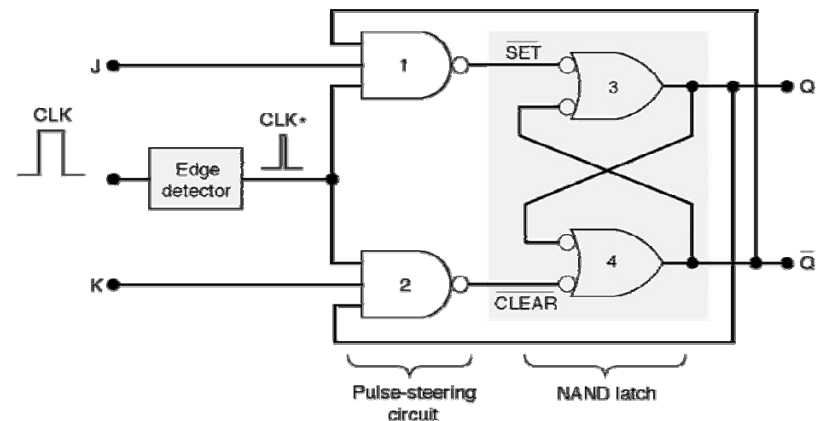
Clocked J-K FF

(a) Clocked J-K flip-flop that responds only to the positive edge of the clock; (b) waveforms.

(a)

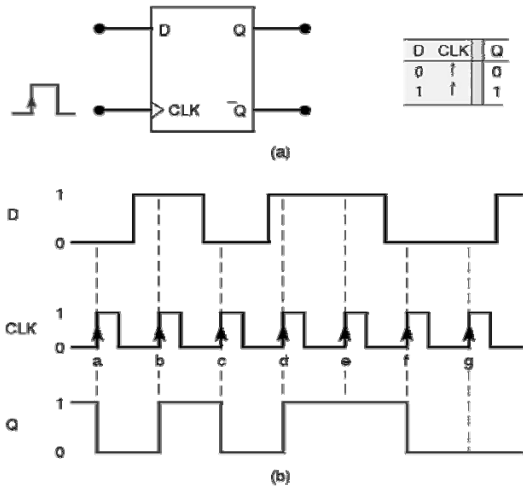J=K=1 condition does not result in an ambiguous output

(b)

Internal circuitry of edge-triggered J-K flip-flop

Clocked D Flip-Flop

D FF that triggers only on positive-going transitions; (b) waveforms.

(a)

D	CLK	Q
0	↑	0
1	↑	1

(b)

Clocked D Flip-Flop from J-K Flip-Flop

(a)   ≡   (b)
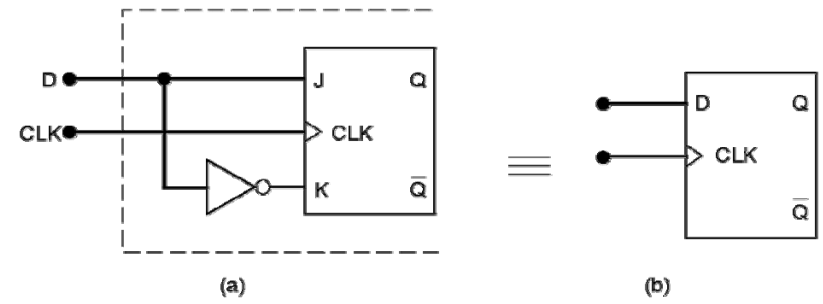
Parallel Data Transfer using D-FF

$Q_1 = X^*$

$Q_2 = Y^*$

$Q_3 = Z^*$

*After occurrence of NGT
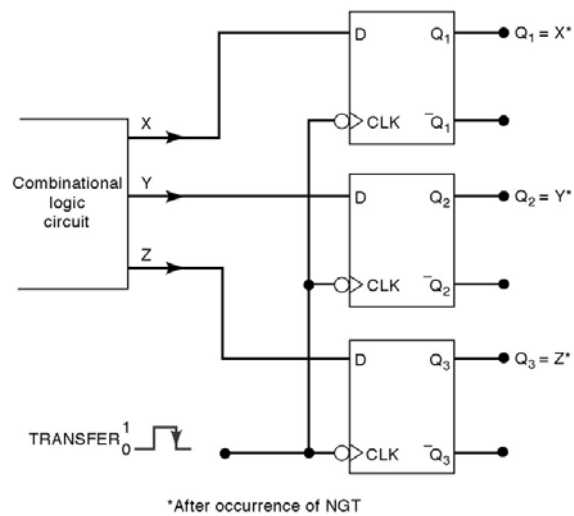
D Latch (transparent latch)

NAND LATCH

(a)

Inputs		Output
EN	D	Q
0	X	Q_0 (no change)
1	0	0
1	1	1

"X" indicates "don't care"
Q_0 is state Q just
prior to EN going LOW

(b)

(c)
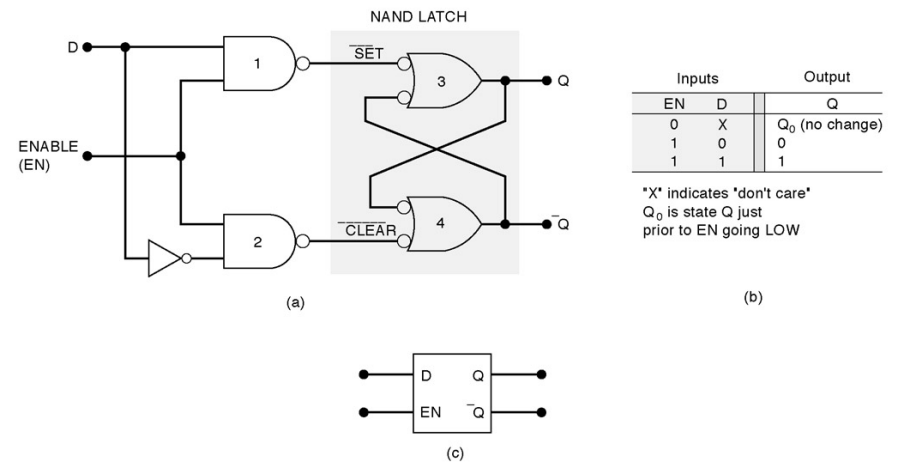
Transparent Latch Timing

EN

D

Q

| T_1 | T_2 | T_3 | T_4 |

"Latched" at Q = 0   "Transparent" Q = D   "Latched" at Q = 1   "Transparent" Q = D   "Latched" at Q = 0
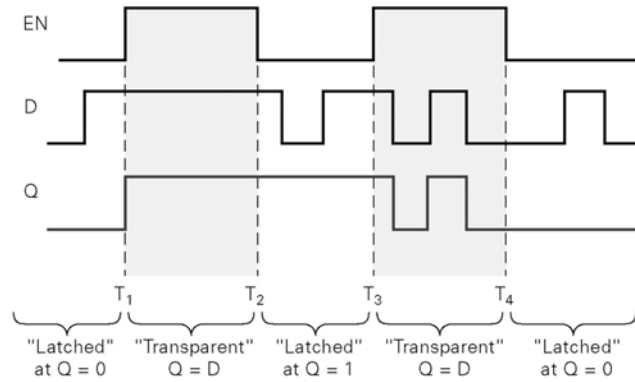
Asynchronous Inputs to FF

The S, C, J, K, and D inputs is called synchronous inputs because their effects on the output are synchronized with the *CLK* input.
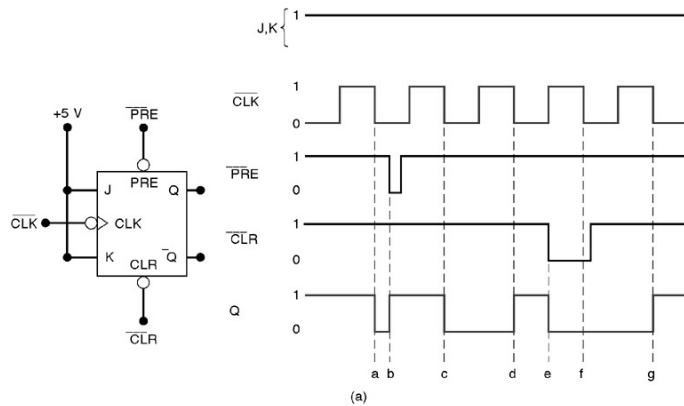
Asynchronous inputs (override inputs) operate independently of the synchronous inputs and clock and can be used to set the FF to 1/0 states *at any time.*
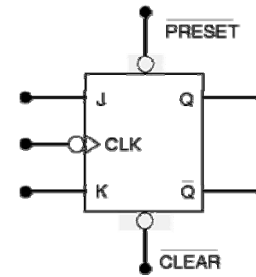
PRESET	CLEAR	FF response
1	1	Clocked operation*
0	1	Q = 1 (regardless of CLK)
1	0	Q = 0 (regardless of CLK)
0	0	Not used

*Q will respond to J, K, and CLK

Asynchronous Inputs cont.

(a)

Point	Operation
a	Synchronous toggle on NGT of CLK
b	Asynchronous set on PRE = 0
c	Synchronous toggle
d	Synchronous toggle
e	Asynchronous clear on CLR = 0
f	CLR over-rides the NGT of CLK
g	Synchronous toggle

(b)