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Analysis of sidewall quality in through-wafer deep reactive-ion etching

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Abstract

The quality of channel sidewalls resulting from through-wafer deep reactive-ion etching is analysed using scanning electron microscopy, atomic-force microscopy and interferometry. Sidewall quality and profile are highly dependent on the width of the etched channel. Channels narrower than 100 μm show generally good sidewall smoothness, though with a bowed profile. This profile leads to ion-induced damage towards the bottom of the channel sidewall. Wider channels, in contrast, exhibit overpassivation of the sidewalls with a region of thick polymer build-up followed by vertical striations and a very rough surface, but with an overall vertical profile. Redeposition of the passivation from the trench bottom to the sidewalls as suggested by other researchers is supported by our observations.

Keywords: Deep reactive-ion etching; MEMS; Fluorocarbon redeposition; Sidewall morphology

1. Introduction

High-aspect-ratio (defined as the ratio of width to depth) structures fabricated from silicon are finding application in a variety of devices ranging from gyroscopes, accelerometers and optical switches to interconnect technology [1,2]. Particularly, through-wafer etching is being used to maximize aspect ratios and provide vias between the die surfaces. Deep reactive-ion etching, most commonly the Bosch process [3,4], is the technique of choice for through-wafer etching of holes and trenches. The vertically directed ion bombardment of classic reactive-ion etching is repeatedly interrupted by passivation periods, which coat the sidewalls and trench bottom with a thin layer of polymer. During etching the trench bottom polymer is preferentially removed, followed by a short isotropic silicon etch. The resulting sidewalls should be near vertical, reflecting an overall balance between the etching and passivating steps, but with a scalloped appearance due to alternating etch and passivation cycles.

The vertical etching rate has been found to be dependent on the aspect ratio of the etched features. In general etch 'lag' is seen in narrower etched regions, which do not etch as fast as more open structures [5]. In order to minimise overetching of more open features, masks are often

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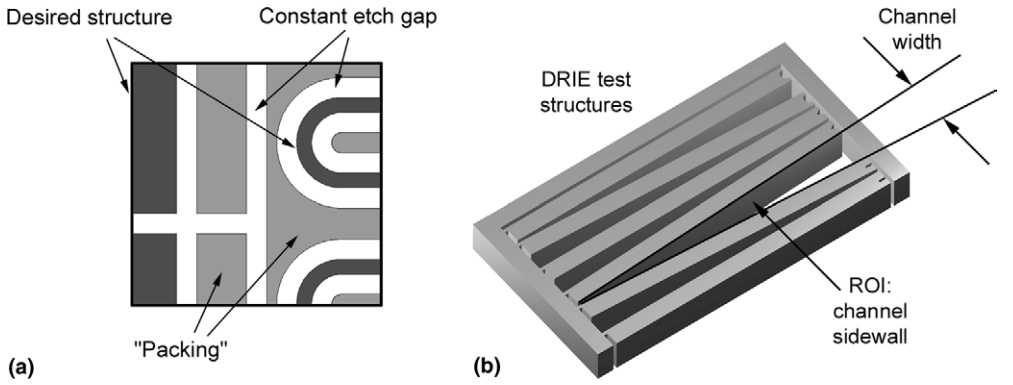

Fig. 1. (a) "Halo" mask design to maintain constant channel width for optimised etching. After through-etching the "packing" pieces fall-out leaving the desired structure, and (b) schematic of test structure showing region of interest (ROI). A tapered channel was selected to examine sidewall surface quality with varying channel width. The individual structures (beams) can be separated for ease of measurement.

patterned as 'halo' geometries [6], with all etching occurring in constant-width trenches, Fig. 1(a).

The aim of this work is to examine sidewall quality as a function of trench width for through-wafer etching, using scanning electron microscopy (SEM), optical metrology, and atomic-force microscopy (AFM).

2. Experiment

Test structures consisting of a series of beams separated by laterally tapered channels, were etched in 525-μm-thick silicon (1 0 0) wafers, Fig. 1(b). The etch pattern was developed in a 15 μm resist mask (AZ9260, Clariant) and the wafer mounted on a Silicon backing wafer using a thermal couplant (Coolgrease, AI Technologies). The DRIE process parameters are shown in Table 1.

After through-wafer etching, the beams were cleaved out of the structure to allow for examination using SEM, AFM, and white-light interferometry.

The SEM was a LEO 1450 VP (Leica Electron Optics) operated at 30 kV, incorporating Oxford Instruments Energy Dispersive X-ray (EDX) spectrometer for elemental analysis.

A Nanosurf Easyscan AFM was used to image the sidewalls at selected points along the etched beams, particularly the scalloped regions visible within 15 μm of the top surface. All measurements were done in dynamic mode, with Silicon tips. Scan areas were typically 50×50 μm at scan speeds of 25–50 μm per second.

Table 1

Etch parameters	
Etch#	1
Etch:pass time (s)	11:8
$SF_6 + O_2$ flow rate (sccm)	130 + 13
$C_4F_8 + O_2$ flow rate (sccm)	85 + 0
Etch time (min)	275
Platten power (W)	20
Coil power (W)	600
Pressure (etch/pass) (mTorr)	20/11
APC angle (%)	74
Etch depth (μm)	525
Etch rate (μm/min)	1.90
Etch:pass ratio	1.375
SF_6:C_4F_8 flow ratio	1.53

In order to examine the topography quantitatively over large areas, a scanning white-light interferometer (ZYGO Newview 200) was used for non-contact mapping of the etched surface.

3. Results and discussion

The DRIE parameters were chosen to give initial near-vertical sidewalls. Fig. 2(a) shows an SEM image taken after 70 μm of etch. Both narrow and wide trenches show approximately the same sidewall geometries, although a build-up of

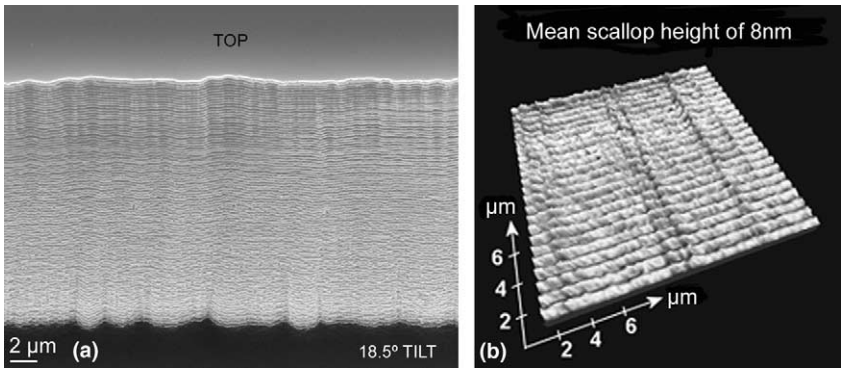

Fig. 2. (a) Scalloping is clearly visible for "shallow" DRIE etches. The sample has been cleaned in Pirhana etch (H_2SO_4:H_2O_2, 3:1) before imaging to remove any residual fluorocarbon film, and (b) AFM scan of top edge showing scalloping through thick polymer coating at wider channel width.

passivation is evident as the trench widens. An AFM image shows the scalloping at the top of the trench, Fig. 2(b).

Fig. 3 shows the sidewall from one side of a low-angle laterally tapering channel etched completely through a 525-μm silicon wafer. The channel thickness in this image varies from 40 to 300 μm, with a taper angle of 6°. Overall, the sidewall is smoothest at the narrower end of the channel, although puncturing of the sidewall with micrometer-sized holes is evident towards the bottom. No scalloping is seen at the narrower end of the channel for the entire depth of the sidewall. As the channel widens to greater than 100 μm, vertical striations increasingly emerge, resulting in a columnar appearance for the lower portion of the sidewall. At wider channel width areas of complete sidewall breakdown occur from about 50 μm down. Optical profilometry using white-light interferometry shows that at the narrower channel width, bowing of the sidewall occurs as shown in Fig. 4. A cross-section of the sidewall shows that the re-entrant surface emerges towards the bottom. In contrast, for wider channels, the profile is near vertical although the roughness of the sidewall towards the bottom prevents interferometric measurement.

Considerable damage is evident over much of the bottom edge of the beam. This is due to non-uniform electrical field at the wafer-coolgrease interface deviating the ion flux laterally. The damage is further increased due to the overetching required to make sure the wafer is etched in slow-etching narrower channels.

For good-quality DRIE, etching and passivation should remain in balance at the sidewalls throughout the etch, although etching should dominate at the trench floor. We will analyse these results in terms of this balance. For the sidewalls, if etching dominates, the sidewall polymer will be removed

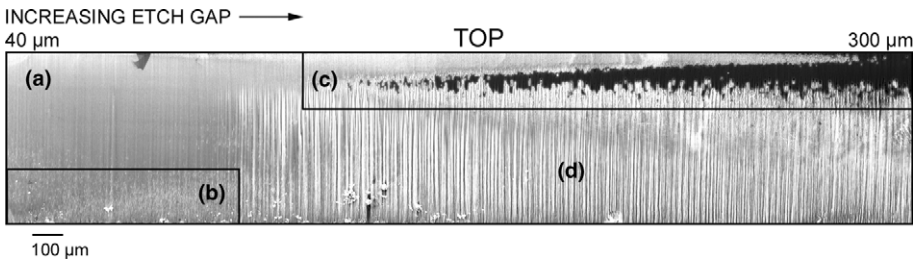

Fig. 3. Sidewall SEM of through-wafer deep reactive-ion etched beam. Zones of varying sidewall morphology are labelled as: (a) overetched; (b) ion damaged; (c) overpassivated; (d) striations.

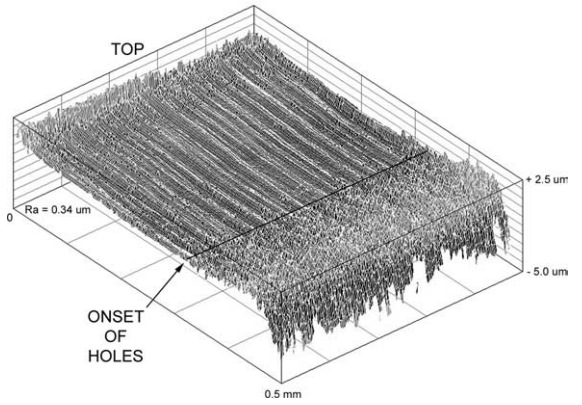

Fig. 4. Interferometric measurement of sidewall topography near narrow channel end. The ion bombardment causes holes in the sidewall near the channel bottom where the re-entrant surface emerges above the top edge.

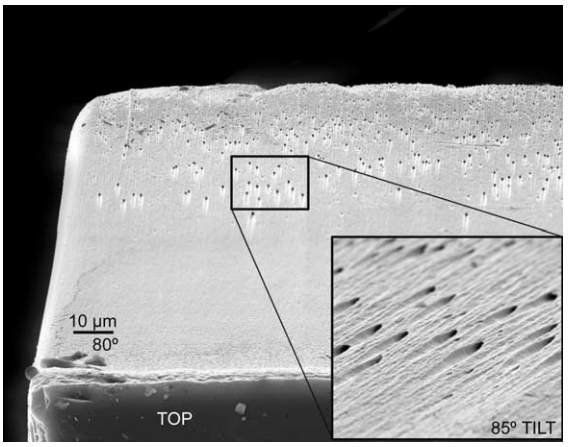

Fig. 5. SEM picture showing the damage observed at narrow etch-gaps towards the channel bottom caused by ion bombardment (inset: zoomed, rotated view at a tilt angle of 85°).

allowing subsequent Silicon etching with the slow erosion of the initial scalloping. If passivation dominates, the polymer layer will thicken with time, being thickest towards the top of the sidewall.

The loss of scalloping of the sidewalls for the smaller channel width can now be seen as a result of overetching. Bowing often accompanies such overetching [5]. The major problem for this portion of the sidewall is the damage towards the bottom of the sidewalls. Combining the SEM images of the distribution of this damage with the optical profilometer data shows that the onset of damage occurs as the re-entrant surface emerges from under the top surface of the wafer. Low-angle SEM imaging shows these holes are circular as viewed vertically downwards, Fig. 5. The probable cause of this damage is therefore low-angle ion-etching of the sidewall.

At larger channel widths, passivation dominates. Fig. 6(a) shows in detail the build-up of polymer at the top of the sidewall of the through-etched wafer. Energy dispersive X-ray micro-analysis confirmed the fluorine content of this layer, Figs. 6(b)–(d). The scalloping is evident under the polymer, as is the onset of sidewall breakdown 100 μm from the top. A portion of polymer has detached from the sidewall, showing that the thicker passivation itself evolves into a non-uniform film. Sidewalls below passivation breakdown show the onset of vertical striations.

Charging in the SEM, evident as pale borders at the polymer edges, is suggestive of a polymer-film breakdown in the DRIE. It is known that charging of the polymer film disrupts the ion flux during the etch step [7]. Polymer build-up appears to reach a critical level at which charging is unstable with respect to lateral uniformity of the process. Hence overpassivation rather than overetching results in a much lower-quality sidewall.

To understand these results we have to answer two questions. What causes the transition from overetching to overpassivation of the sidewalls with increasing trench width? And for the narrower trenches, what causes a transition to overetching of the sidewalls with increased trench depth? In both cases, an increase in passivation, a reduction in etching or a combination of both could be responsible. The two questions can be combined into a single question – what causes an increased passivation or reduced etching of the sidewalls for lower aspect-ratio trenches? In the discussion that follows, it is assumed that the gas pressure is in the rarified regime, where gas–gas collisions can be neglected and diffusion cannot occur.

The passivation layer consists of single-chain carbon difluoride polymer. As the carbon–carbon and carbon–fluorine bonds are two of the strongest bonds in organic chemistry, considerable energy is required to either grow or shorten the polymer chains. For growth, a combination of

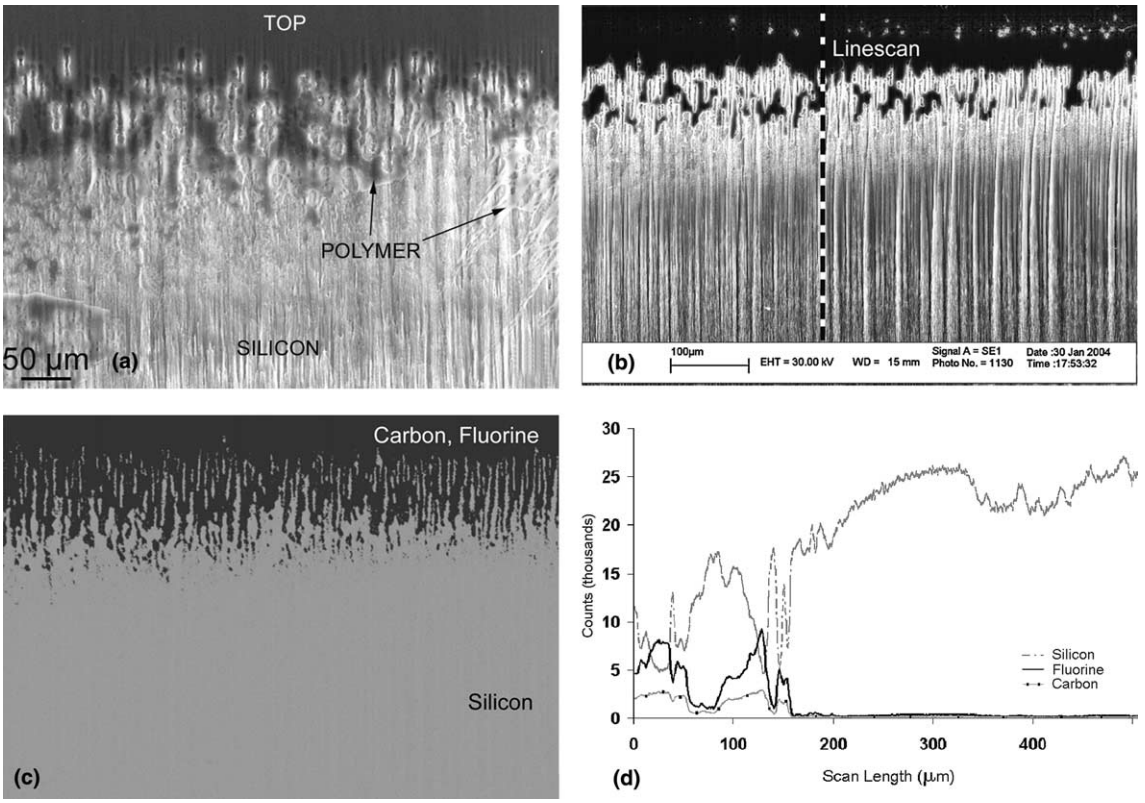

Fig. 6. EDX analysis of the beam shows fluorine presence in the darker areas that were charging up in the SEM, proving the hypothesis of CF_2 deposition: (a) passivation build-up observed at wide etch-gaps leading to striations and therefore to rough sidewalls; (b) SEM image of the beam section analysed for fluorine content; (c) elemental map of the beam highlighting (black) the carbon and fluorine dominated regions; (d) linescan from the top edge of the beam to the bottom edge showing the concentration of fluorine, carbon and silicon along the etch direction.

ions and fluorine radicals is required to dislodge a fluorine atom from the chain. CF_2 radicals, essentially PTFE monomers, can then add to the chain, with the final addition of a terminating fluorine radical [8]. For reduction of the chain, the process is reversed, and the polymer is etched. High-energy vertically directed ions are present during the etching steps, while during passivation, when the accelerating voltage is zero, lower-energy ions are scattered isotropically from the plasma. The equilibrium position of the growth/etch reaction is determined by the incoming flux of CF_2 radicals and ions.

At the floor of the trench, there will be an incoming flux of CF_2 radicals during the passivation step. Before any silicon etching can take place during the etching step all the polymer deposited on the floor during the passivation step must be removed, again as CF_2 radicals. Redeposition of the polymer from the trench bottom to the sidewalls has been identified as a substantial contribution to sidewall passivation in previous work [9–13]. Analyses and experimental data have indicated that the incoming flux of CF_2 radicals as etching products will vary at different heights of the trench sidewall [13] and there will be a reduced, lower-incident-angle flux of CF_2 radicals towards the top of the sidewalls and less redeposition of polymer.

This provides an explanation for the etching of the passivation towards the top of the sidewalls at narrower channel widths. The flux of redeposited CF_2 is reduced as the trench is etched, causing the polymer thickness deposited on the sidewall over an entire cycle to be less than the thickness etched,

inevitably leading to eventual overetching of the sidewalls. Overpassivation of the sidewalls at wider channel widths can be explained by the increased flux of CF_2 radicals from the broader floor of the trench as more material is etched from the floors of the wider trench. The passivation in this case grows more than it is etched during each cycle, causing build-up of passivation beyond a critical level for uniform coverage.

Although redeposition of etched passivation provides an explanation consistent with observations, other effects could contribute. During the passivation step, the flux of activating ions at sidewalls might be expected to drop with trench depth. However, the flux at the top of the sidewalls would be the same for all channel widths, whereas a transition from overetching to overpassivation is observed. Therefore, ion-flux variations during the DRIE cycles are unlikely to provide a complete explanation.

4. Conclusions

We have tried to simulate conditions, which give rise to various sidewall surface defects in the same test sample to analyse it thoroughly with different test and measurement equipments.

Sidewall quality of through-wafer DRIE structures is very dependent on the aspect ratio of the etched channels. Below about 100 μm etch width, sidewalls tend to be smooth, albeit overetched, with some bowing leading to ion damage towards the bottom of the sidewalls. For wider channels build-up of passivation leads to an eventual breakdown in polymer coverage, causing vertical striations and a very rough surface.

This behaviour is analysed as a transition to overpassivation for increased channel width, and a transition to overetching with etch depth for the narrower channels. Redeposition of passivation from the trench floor during the etch step is suggested as an explanation in both these regimes.

As the aspect ratio of the trenches changes during etching, no single set of process parameters can be expected to optimise the balance between sidewall passivation and etch for a through-wafer etch. Ramping of parameters may be one route to improved sidewall quality.

For the used process parameters a channel width of 40 μm for "halo" mask design seems to ensure smooth and straight sidewalls in through-wafer deep reactive-ion etching.

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